Amendments to the Specification

Please replace the paragraph on page 3, lines 10-17 with the following amended paragraph:

In the general twin-cell DRAM disclosed in the prior art 1 or the like, the refresh interval can be longer than that in the single-cell DRAM. In recent years, however, semiconductor devices have been employed in an increasing number of portable devices primarily powered by batteries, and therefore demands for reduction of the size and power consumption of the semiconductor memory devices have been increasing. Thus, the twin-cell DRAM is likewise required to increase further the refresh period, and thus to improve further the refresh characteristics.

Please replace the paragraph on page 9, lines 4-15 with the following amended paragraph:

Storage node contacts 170 in each column are located at positions corresponding to every two rows, and storage node contacts 170 in each row are arranged at positions corresponding to all the columns [[rows]] except for the row at the end position. The rows, in which bit line contacts 160 are arranged, alternate with the rows of storage node contacts 170. Word lines WL extend across field regions 200, and are arranged such that bit line contacts 160 and storage node contacts 170 are located between word lines WL. Fig. 2 representatively shows word lines WL0 - WL7. In the whole memory cell array, the layout shown in Fig. 2 is repeated in the row and column directions. In the figures, "F" indicates a minimum design unit (minimum line width).

Each of the word and bit lines has a with equal to F, and the word and bit lines are arranged at pitches each equal to F.

Please replace the paragraph on page 16, lines 26-30 with the following amended paragraph:

These dummy word lines DWL [[WDL]] are formed in the same interconnection layer as word lines WL, and are produced in the same manufacturing steps as word lines WL. Therefore, dummy word lines DWL can be arranged without an additional manufacturing step and an additional mask.

Please replace the paragraph on page 21, lines 3-13 with the following amended paragraph:

For example, as shown in Fig. 13, isolated cell plate 130# may be arranged for each memory cell row in the layout according to the first embodiment shown in Fig. 2. In this case, each isolated cell plate 130# can be shared by a plurality of (two in Fig. 13) twin-cell units belonging to the same memory cell row ~~column~~. For this arrangement, however, it is essential that the voltages on the storage nodes storing the complementary data in each twin-cell unit vary within a similar range owing to the capacitive coupling. These voltage variations are caused by suppressing the capacitance of each isolated cell plate. Therefore, the effect of the invention is remarkably achieved by isolating the cell plate for each twin-cell unit.